SYSTEMS ENGINEERING BULLETIN

NUMBER	SEB-00-03-001
VERSION / ISSUE	1.0
DATE	March 2000
SUBJECT	Capacity Limitations in XPM13 with SX05
DESCRIPTION	This document describes the Capacity Limitations of DMS-100MMP XPM/CPM products with the SX05 processor
CONTACT	MMP Capacity and Performance Engineering
MARKET	MMP

Kevin Yong
Capacity and Performance Engineer
Alpha Introductions to Market
Nortel Networks

Ian Turner
Manager
Alpha Introductions to Market
Nortel Networks

**DMS is a trademark of Nortel Networks plc.*

TABLE OF CONTENTS

1 INTRODUCTION ... 3
2 CAPACITY CONSIDERATIONS ... 4
2.1 Grade of Service ... 4
2.2 Processor Utilisation ... 4
2.2.1 Idle Occupancy ... 5
2.3 C-side messaging limitations ... 6
3 CALL EVENT CAPACITIES ... 7
4 PROCESSOR UTILISATION CALCULATION ... 10
5 GLOSSARY ... 13
6 REFERENCES ... 14
APPENDIX A - XPM CAPACITY CONCEPTS ... 15

1 INTRODUCTION

This document covers the real time performance gain of the SX05 PowerPC processor (referred to hereafter as the **SX05**), which is available for the DTCO, DTC2 and GPP DMS-100 peripherals as of MMP13. Customers should contact their Business Unit Sales Engineers for any assistance required with this SEB.

These guidelines may be used for all new and existing DTCO, DTC2[1] and GPP peripherals when provisioned with the SX05. Future versions of this document will include any other peripherals that use the SX05.

The SX05 has been introduced to succeed the MX77 unified processor (UP), which is currently available as standard in most peripherals. As of MMP13, the SX05 will be baseline hardware for the DTC2 peripherals, and available as a faster alternative processor for the DTCO and GPP peripherals. Eventually, the SX05 will be baseline in both of these peripherals (currently planned for MMP17), and it is also planned for use in the DTCOi, LGCO and LGCOi peripherals (MMP15).

Current forecasts indicate that the SX05 will process call events 10 times faster than the MX77, hence eliminating this processor as the capacity 'bottleneck'. However, this does not mean that the overall capacity of the peripheral will increase ten fold. This document has been written to explain the other possible bottlenecks and to provide some guidelines for calculating actual peripheral capacity. A Capacity Planning Tool for the GPP is also available from Sales Engineers that allows you to forecast the impact on capacity of upgrading the software load or changing the traffic mix.

This document will use Call Events per second (CE/s) as the measure of capacity (cf. Appendix A for more details on call events). Call timings, given in milliseconds (ms), and guidelines for calculating processor utilisation will also be included for the GPP, along with details of other capacity limiting 'bottlenecks'.

Please note: this version of the SEB does not include GPP and DTCO measurements. These will be included as soon as they become available. Please contact the author for more assistance

[1] DTC2 refers to both DTCO2 and DTCO2i peripherals

2 CAPACITY CONSIDERATIONS

There are three main areas that should be taken into account when engineering all peripherals:

- Grade of Service
- Processor utilisation
- C-side messaging limitations

This chapter will cover each factor, explaining their part in capacity planning.

2.1 Grade of Service

Grade of Service, in its simplest terms, refers to the number of blocked calls that you are prepared to encounter when processing calls. For example, a Grade of Service of 0.001 translates to 1 blocked call in every 1000.

For each Grade of Service the amount of traffic (measured in Erlangs) is then calculated to ensure that this blocking ratio is met. Traffic Tables are available that allow you to simply look up the Erlang throughput that can be presented for a given number of channels (for more information contact your Sales Engineer)

Example: for 480 channels engineered to a Grade of Service of 0.001, a maximum of 423.63 Erl of traffic can be carried during the Busy Hour (see **Table 2.1**)

Table 2.1: DS-512 Erlang Capacity

GOS	Erlangs Carried	GOS	Erlangs Carried	GOS	Erlangs Carried	GOS	Erlangs Carried
0.06	461.25	0.04	456.97	0.02	449.72	0.005	436.44
0.05	459.33	0.03	453.94	0.01	442.83	0.001	423.63

2.2 Processor Utilisation

Generally with most peripherals (and in fact the CM), the limitation to capacity is the processor. Several projects have been working on this, one of which is the SX05 introduction. In the past, the MX77 proved to be the bottleneck on all the peripherals in which it was installed (except in cases of extreme traffic engineering, when the Grade of Service was the issue). For the DTCO, DTC2 and GPP, this bottleneck can now be removed with the SX05, though for GPP and DTCO2i the bottleneck is moved to the EISP (Enhanced ISDN Signal Processor).

The SX05 Processor real time is split into three areas:

- Buffer - assigned headroom designed to protect Grade of Service during periods of peak traffic.
- Call Processing - assigned for call processing. The size of this area is dependent on the size of the Idle Occupancy. It is recommended that Utilisation of this area does not exceed 80% for the DTCO and DTC2, and 90% for the GPP.
- Idle Occupancy - taken up by background processing (see **2.2.1**).

Figure 2.1: Processor Allocations

Buffer (allocated ~ 20%)
Call Processing (calculated)
Idle Occupancy (measured)

2.2.1 Idle Occupancy

Idle Occupancy is the processor time used for background processes - SWACT co-ordination, maintaining integrity, messaging, maintenance etc. It is measured on a fully configured[2] peripheral when no calls are being processed, and so is sometimes also known as No Load Occupancy (NLO). Where peripherals are not fully configured, the actual Idle Occupancy can be lower than the NLO. This difference is negligible for the DTCO and DTC2 peripherals, but needs to be quantified for the GPP.

For the DTCO2 and DTCO2i peripherals the Idle Occupancy for the both the SX05 and EISP (DTCO2i only) has been measured at 7%.

Measurements for the GPP and DTCO were not available at time of going to print. Please contact the author for further assistance.

[2] 'Fully configured' means that the peripheral is provisioned with the maximum number of E1s (16 for the DTC and DTC2, 24 for the GPP).

2.3 C-side messaging limitations

The DTCO, DTC2 and GPP peripherals all connect back to the DMS core via single DS-512 links. 480 channels of these links are used to carry traffic, whilst the other 32 channels are used for messaging. In the past, the MX77 processor proved to be the capacity bottleneck, with the processor going into overload before any other limitation was experienced. However, with the introduction of the SX05, this bottleneck has been removed, leading to the exposure of other capacity bottlenecks such as C-side messaging.

The amount of C-side messaging depends on the number of simultaneous call events that originate and terminate at the peripheral. Once the number of generated messages exceeds the C-side limitation, the peripheral either goes into overload or 'C-side busy' state.

Details on the maximum number of call events that can be handled are given in **Chapter 3**.

3 CALL EVENT CAPACITIES

3.1 DTCO2 and DTCO2i

For the DTCO2 and DTCO2i the following call models were used to simulate the typical traffic originating and terminating on these peripherals:

Table 3.1: UK and International DTCO2 call models

Call Type	UK model	Int'l model
ETSI ISUP V1	24%	30%
ETSI ISUP V2	16%	30%
ANSI ISUP	20%	30%
BTUP	32%	0%
UK ISUP	8%	0%
ISUP Variant	0%	10%

Table 3.2: International DTCO2i call model

Call Type	Int'l model
DPNSS	40%
PRI	40%
Swiss PRI	20%

The call event capacity of each peripheral is measured using these traffic models, with the following results:

Table 3.3: DTCO2 Call event capacities

		CE/sec	SX05 occupancy	
			Terminations	Originations
UK	**Call overflow**	13	18%	19%
	Peripheral Overload	14	18%	19%
International	**Call overflow**	14	18%	18%
	Peripheral Overload	15	19%	19%

Table 3.4: DTCO2i Call event capacities

		EISP Occupancy level	Terminations		Originations	
			CE/sec	SX05 Occ.	CE/sec	SX05 Occ.
International	**ECL for EISP**	80%	23	34%	21	24%
	Peripheral Overload	100%	30	40%	30	30%

Table 3.3 shows the call event capacities for the two DTCO2 call models. For this peripheral with the SX05 processor, the capacity limitation is due to the C-side messaging limitation. Hence, even though the Processor Occupancy does not exceed 19% for both call models, the peripheral can only handle around 13 CE/s before calls start to overflow. This is equivalent to around 50 calls per circuit per hour, or all trunks fully utilised with an average Call Hold Time of 74 seconds[3], which should prove to be more than sufficient for the majority of customers.

On the other hand, **Table 3.4** shows that for the DTCO2i the bottleneck is in fact the EISP, the other processor in the peripheral. At the Engineered Capacity Limit (ECL) of 80% for the DTCO2i, the EISP can process 23 terminating or 21 originating call events for this call model. For a mix of terminating and originating call events use a weighted average:

CE/s = (23 Terminating CE/s x Terminating %) + (21 Originating CE/s x Originating %)

E.g. If 50% of all call events are terminating then the EISP can process 22 CE/s

[3] The formula for this is Calls per circuit per hour = 3600 x Trunk Occupancy (Erl) / Call Hold Time (sec)

Given these results, it is recommended that the traffic does not exceed **13 CE/s for the DTCO2**, and **21 CE/s for the DTCO2i** as a rule of thumb. There is no need to calculate processor utilisation for the DTC2 peripherals if these rules of thumb are used, hence the call event timings are not provided. If you wish to use call event timings, details on how to calculate a call event timing from a relevant call event capacity are given in **Appendix A**.

3.2 GPP

Capacity measurements were not available at time of going to print. Please contact the author for further assistance.

3.3 DTCO

Capacity measurements were not available at time of going to print. Please contact the author for further assistance.

4 PROCESSOR UTILISATION CALCULATION

The following section presents the detailed methodology to be used for the engineering of the GPP. A 100% V5.2 call model is used for the example. Please note that the example only looks at the SX05. When engineering the GPP it is important to engineer both the SX05 and EISP.

Note: The engineering of the AN (Access Node) is beyond the scope of this document. The AN and LE nodes are engineered independently and therefore we can only assume that the guidelines presented here concerning overall grade of service (GOS) have been adhered to by incoming traffic from the AN.

To ascertain if the GPP's processors can support the intended offered traffic:

Step 1 - Calculate the offered call attempt rate per line for each required signal type in the call model. Then calculate the weighted call attempts for each required signal type in the call model.

Step 2 - Calculate the combined call timing for each required signal type in the call model.

Step 3 - Calculate the call processing area required for the call mix

Step 4 - Calculate the call processing area that is available and the call processing area in milliseconds. Then calculate the total number of all lines that the processor could support.

Step 5 - Calculate the processor utilisation for the required number of lines in the call mix.

For the purposes of this example,

- Traffic level per V5.2 line - 0.1 Erlangs
- Call Hold Time for all V5.2 lines - 180 sec
- 50% of V5.2 lines are V5.2 DT, 50% are V5.2 DP
- Origination/termination ratio for all lines - 50:50 (orig: term)
- 8 AN interfaces - each interface supporting 120 DT lines and 120 DP lines
- Each AN interface connected to GPP via 2 PCM-30 carriers

Note: The above P-Side and C-Side configuration matches Nortel's V5.2 AN the PDMX-EV

4.1 Calculation

Step 1: Calculate the offered call attempt rate per line for each required signal type in the call model and then the weighted call attempts for each required signal type in the call model.

Column	A	B	C	D	E	F
Method				B / C		D * E
	Line Type	Traffic Erlangs per line	CHT(s)	Offered CE/s	% of signal type on GPP	Weighted CE/s
	V5.2 DT	0.1	180	0.00055556	50%	0.00027778
	V5.2 DP	0.1	180	0.00055556	50%	0.00027778

Step 2: Calculate the combined call timing for each required signal type in the call model.

Column	G	H	I	J	K
Method					(H * I) + ((1-H) * J)
	Line Type	% Origination	Orig Call Event Timing (ms/CE)	Term Call Event Timing (ms/CE)	Combined Call timing (ms/CE)
	V5.2 DT	50	117.2[4]	76.8[4]	97
	V5.2 DP	50	141.5[4]	91.3[4]	116.4

Step 3: Calculate the call processing area required for the call mix.

Column	L	M
Method		K * F
	Line Type	Required call processing (ms/sec)
	V5.2 DT	0.02694
	V5.2 DP	0.03233
	Total	0.05927

[4] All measurements used are for XPM09 with MX77. The document will be updated with XPM13 / SX05 measurements once they are available.

Step 4: Calculate the call processing area that is available and the call processing area in milliseconds. Then calculate the total number of all lines that the processor could support.

Column	N	P	Q	R
Method		80% - (26.2% + (0.2 * N))[4]	P * 10	Q / Total Column M
	No PCM-30s	SX05 call processing available (%)	SX05 CP area (ms)	Total of all lines
	16	50.6	506.00	8537

Note: For this example we are only considering the SX05 processor. Both SX05 and EISP will need to be calculated in a real example.

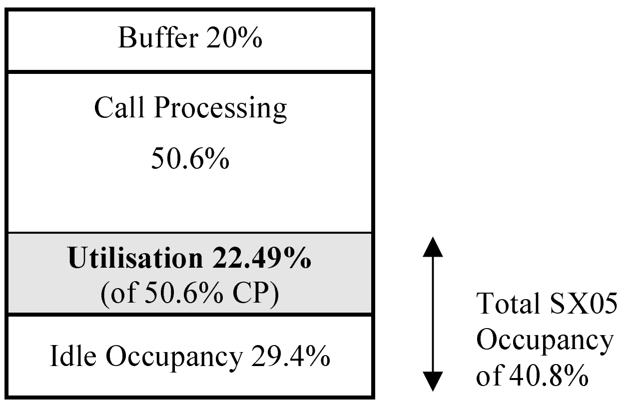
Step 5: Calculate the processor utilisation for the required number of lines in the call mix.

Column	S	T
Method		(Total Column S * Total Column M) / Q
	Total Number of lines	Processor Utilisation (%)
	1920	22.49

Note: The same result for method of column T can be obtained by (Total column S) / R

Diagrammatically the SX05 would be represented by **Figure 4.1**:

Figure 4.1: SX05 processor Allocations



5 GLOSSARY

AN	Access Node
BTUP	British Telecommunications User Part
CCS7	Common Channel Signalling system No. 7
CE	Call Event
CHT	Call Holding Time
CM	Computing Module
DASS2	Digital Access Signalling System No. 2
DMS	Digital Multiplex System
DPNSS	Digital Private Network Signalling System
DTC	Digital Trunk Controller
DTCO	Digital Trunk Controller Offshore
DTCOi	Digital Trunk Controller Offshore ISDN
ECL	Engineered Capacity Limit
EISP	Enhanced ISDN Signal Processor
ENET	Enhanced Network of DMS switch
Interface	Signalling Type (in this context)
ISDN	Integrated Services Digital Network
ISUP	Integrated Services User Part
IUP	Interconnect User Part (previously known as BTUP)
MMP	Multi Market Product
PCM30	Pulse Code Modulation - 30 channels (aka E1)
PDTC	PCM-30 Digital Trunk Controller
PRI	Primary Rate Interface
P-side	Peripheral side (looking out of the switch)
SEB	System Engineering Bulletin
UP	Unified Processor
XPM	eXtended Peripheral Module

6 REFERENCES

[1] SEB 94-01-002 XPM+ Engineering and Administration Guidelines

[2] DMS-100MMP Base Product Description, MMP13

[3] SEB 98-04-005 Performance and Capacity for the DMS-100E GPP at XPM09

APPENDIX A - XPM CAPACITY CONCEPTS

Call Events

Computing Module (CM) call timings are measured for complete calls and capacity recommendations are made on the basis of the maximum number of Busy Hour Call Attempts that can be supported. For peripherals such as DTC this is not possible because a call typically enters the switch on one DTC and leaves on another as shown in Figure A.1 below. The two DTC processors handling the two events need to be treated separately.

The incoming and outgoing call events usually have different processing times, so when calculating call capacity for an interface (signalling type) the split between incoming and outgoing calls on the particular DTC must be taken into account.

The terminology used to describe a half call is that of "Call Event", thus, capacity information for the DTC is expressed as "Call Events/second" (CE/s).

Note: To relate these call capacity values to complete calls they should be halved, for example, for a given signalling type with a call capacity of 6 CE/s then this equates to 3 call attempts per second (3 CA/s).

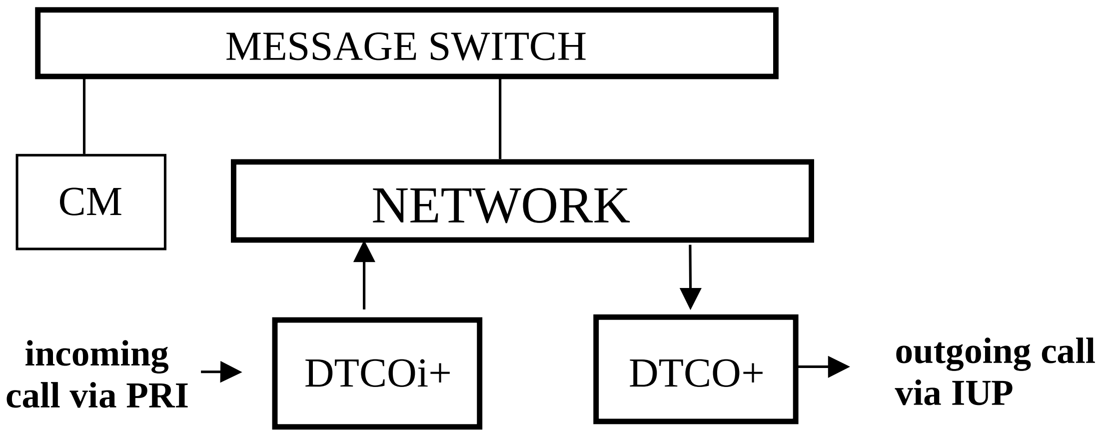


Figure A.1: Peripheral Half Calls

Timings of Call Events

The call event timings for the signalling type are calculated from the measured capacities as follows:

$$\text{Call event timing (ms/CE)} = \frac{\text{Call processing \%}}{100} \times \frac{1000}{\text{Call event capacity (CE/s)}}$$

Having calculated the incoming and outgoing timings, it is possible to work out an aggregate call timing that reflects the proportion of incoming to outgoing calls thus:

Aggregate timing = (i/c timing x i/c proportion) + (o/g timing x o/g proportion).

In most cases, the incoming and outgoing proportions are equal (i.e. 50%), in which case the aggregate call timing is simply the average of the incoming and outgoing timings.